香港中文大學
The Chinese University of Hong Kong

CENG3430 Rapid Prototyping of Digital Systems

Lecture 06: Use of Clock Sources and Peripheral Modules on ZedBoard

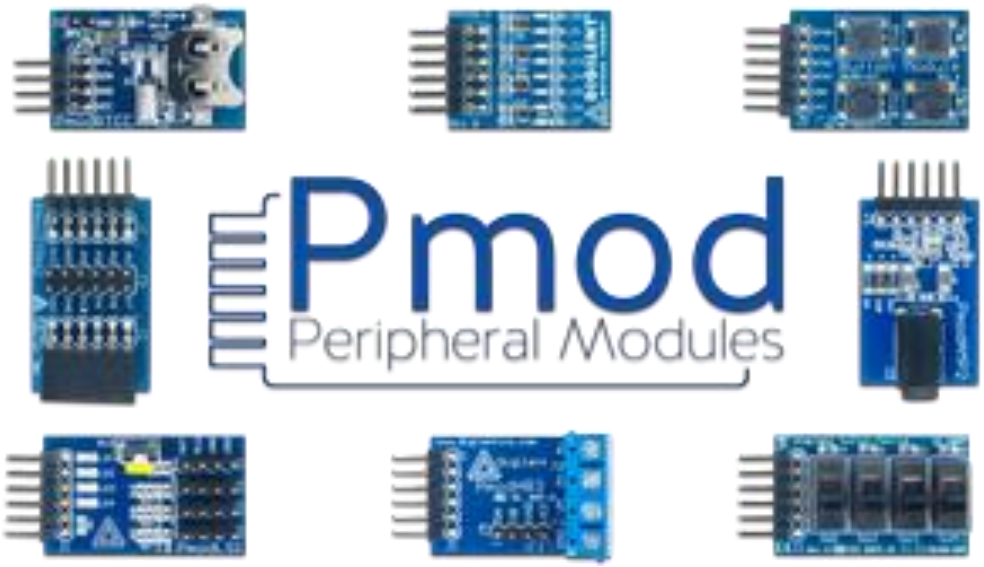
Ming-Chang YANG

mcyang@cse.cuhk.edu.hk

Outline

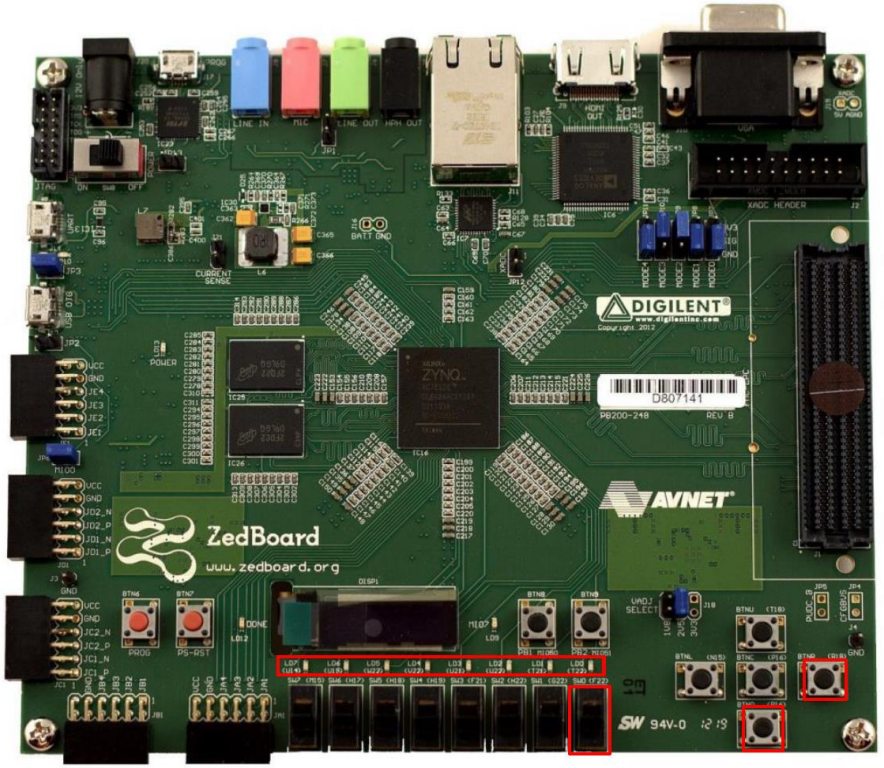
- Clock Sources of ZedBoard

- Digilent Pmod™ Peripheral Modules
  - Example: Seven Segment Display (Pmod SSD)

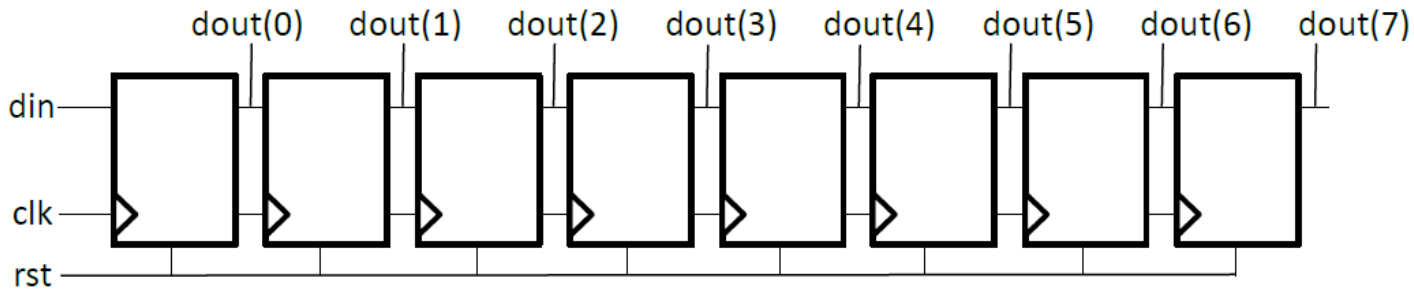


Recall: What we have done in Lab05

- Serial-in-parallel-out Shift Register



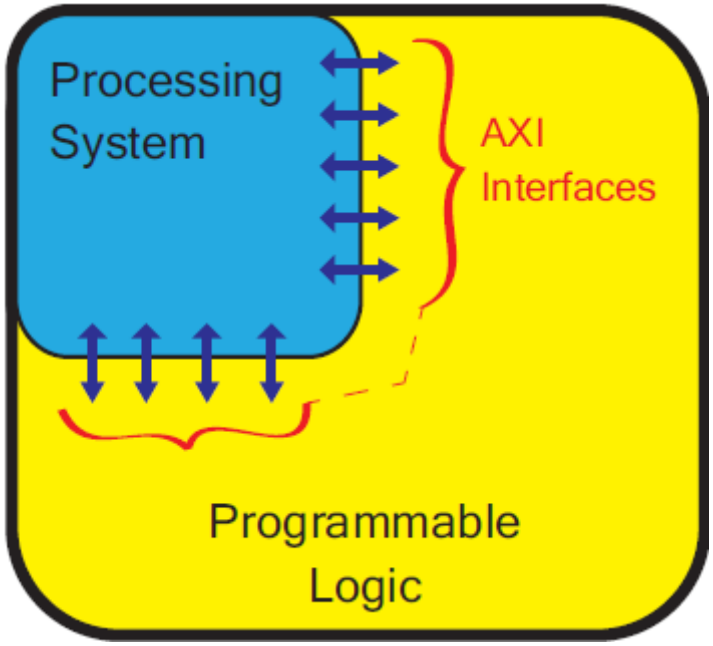
SW0: `din`
BTND: `clk`
BTNR: `rst`
LD0~LD7: `dout`

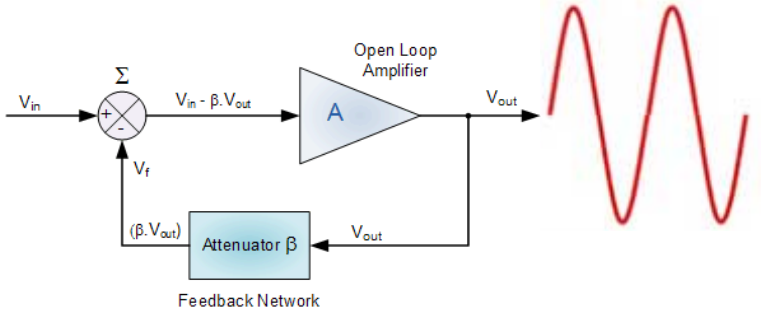


Do we have real clock sources on ZedBoard?

Clock Sources on ZedBoard (1/2)

- **Processing System**
  - PS subsystem uses a dedicated 33.3333 MHz clock source with series termination.
    - IC18, Fox 767-33.333333-12
  - The PS subsystem can generate up to four PLL-based clocks for the PL system.
- **Programmable Logic**
  - An on-board 100 MHz oscillator supplies the PL subsystem clock input on bank 13, pin Y9.
    - IC17, Fox 767-100-136





http://zedboard.org/sites/default/files/documentations/ZedBoard_HW_UG_v2_2.pdf
https://www.electronics-tutorials.ws/oscillator/oscillators.html

Clock Sources on ZedBoard (2/2)

- To use the on-board 100 MHz clock input on bank 13, pin Y9, you need to include the following in your XDC constraint file:

```
set_property IOSTANDARD LVCMOS33 [get_ports clk]
set_property PACKAGE_PIN Y9 [get_ports clk]
create_clock -period 10 [get_ports clk]
```

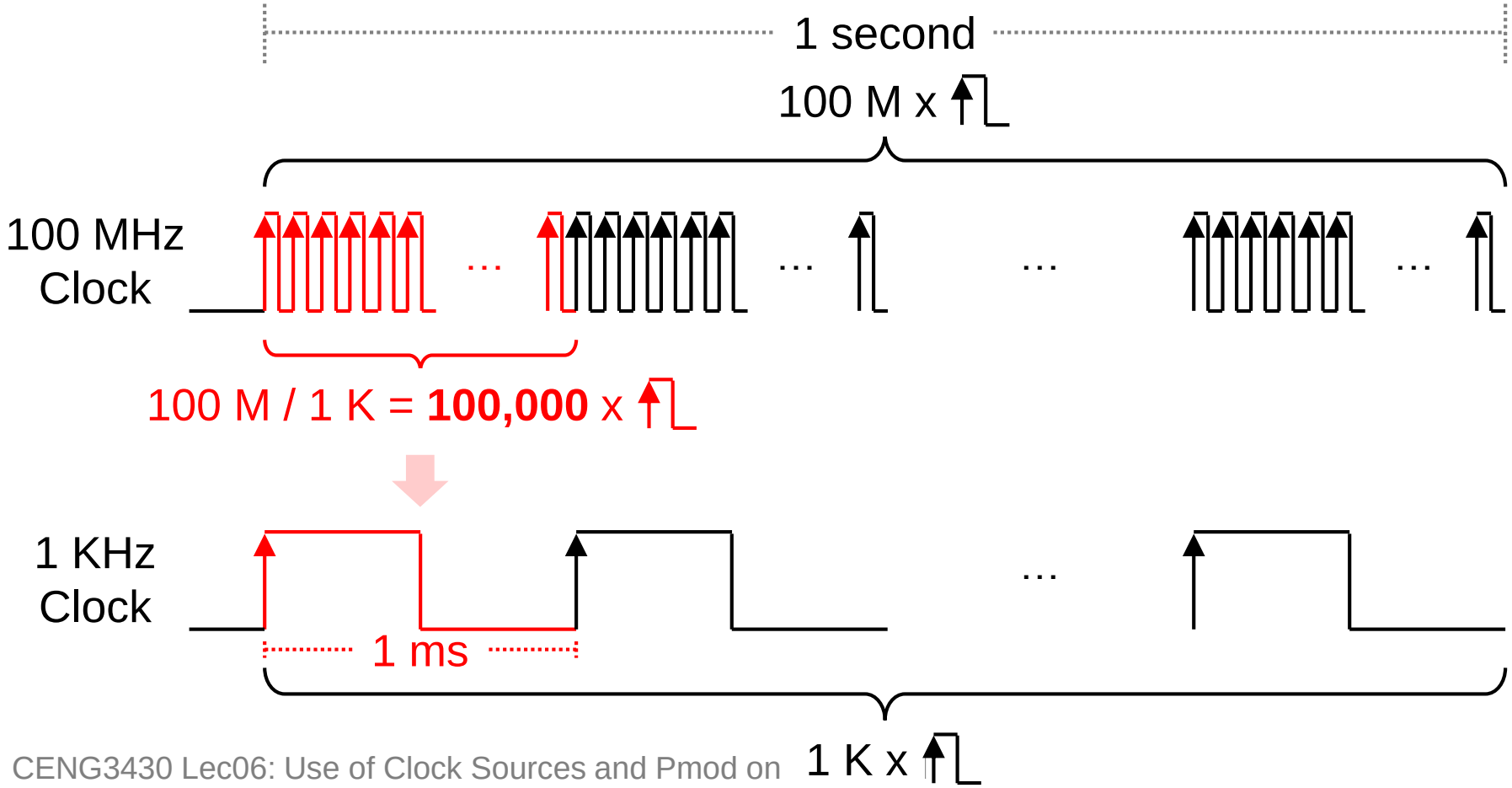
Note:

- *The constraint **`-period 10`** is only used to inform the tool that clock period is 10 ns (i.e., 100 MHz).*
- *The constraint **`-period 10`** is NOT used specify or generate a different clock period from a given clock source.*

http://zedboard.org/content/changing-frequency-clock-using-createclock

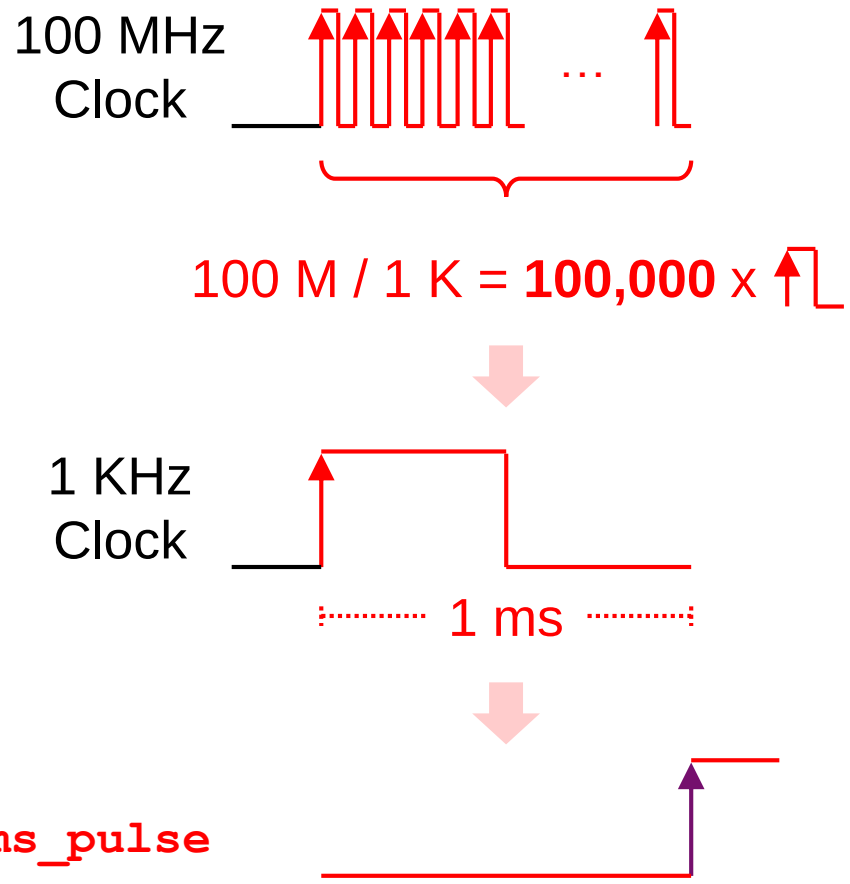
Clocks of Different Frequencies (1/2)

- In practice, we often need clocks of different freq.
- Example: How to create a 1 KHz clock from the on-board 100 MHz oscillator (**`clk`**)?



Clocks of Different Frequencies (2/2)

- **Trick**: If we make a counter (**count**) that counts *n* cycles, then we can generate a pulse (**ms_pulse**) when the counter is at any particular value *n*.




```
signal ms_pulse: STD_LOGIC:='0';
signal count: integer:=0;
process(clk)
begin
  if rising_edge(clk) then
    if (count = (100000-1)) then
      ms_pulse <= not ms_pulse;
      count <= 0; -- reset count
    else
      count <= count + 1;
    end if;
  end if;
end process;
```

Class Exercise 6.1

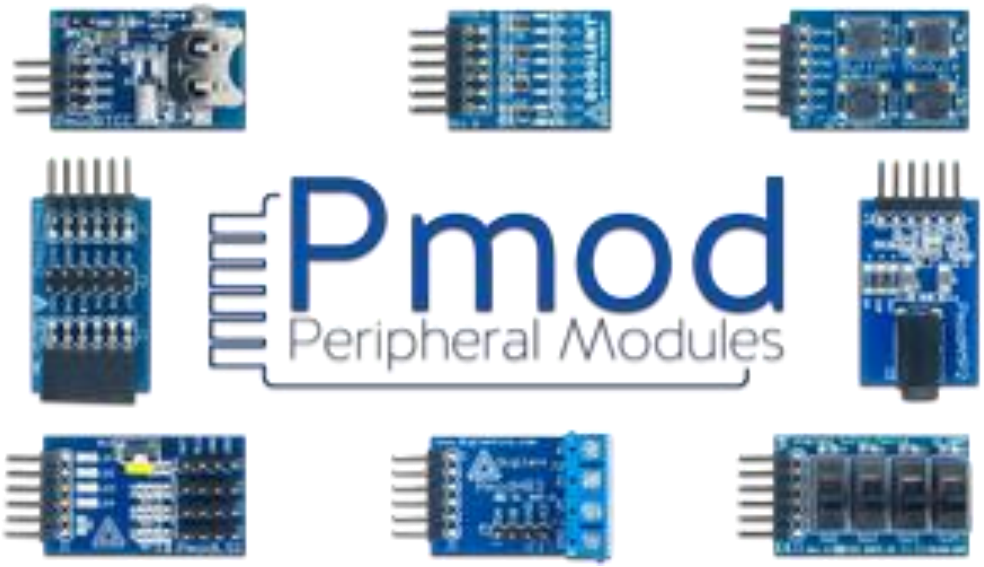
Student ID: _____ Date:
Name: _____ _____

- Write the code to create a 50 Hz clock from the on-board 100 MHz oscillator (**`clk`**).

Outline

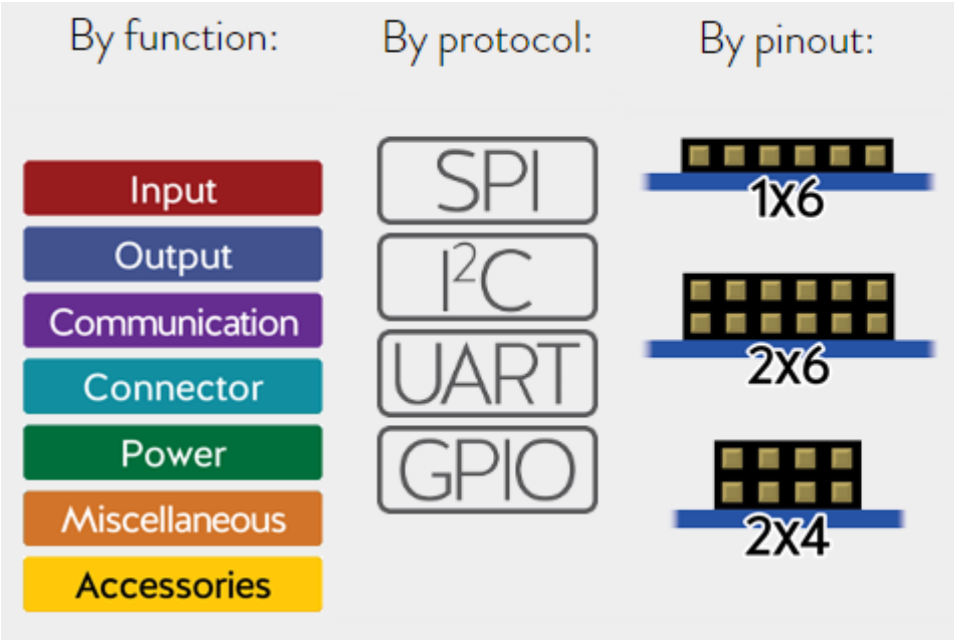
- Clock Sources of ZedBoard

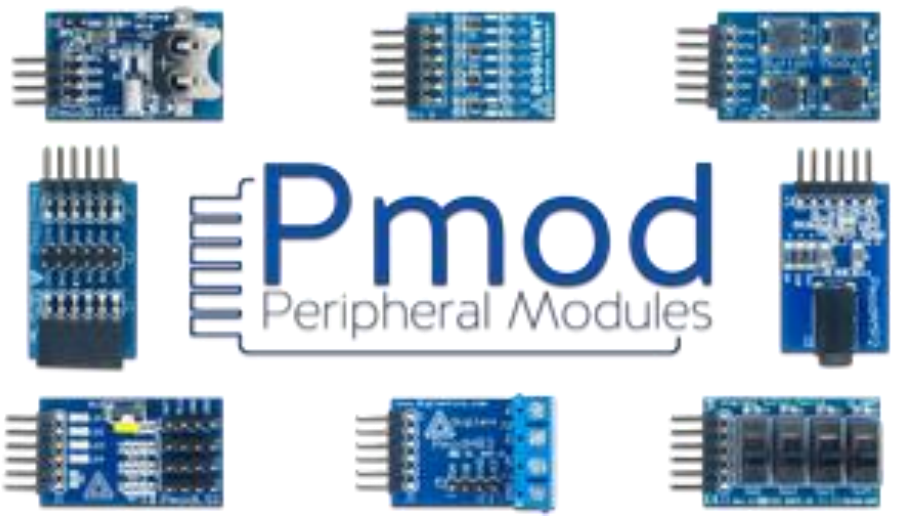
- Digilent Pmod™ Peripheral Modules
  - Example: Seven Segment Display (Pmod SSD)



Digilent Pmod™ Peripheral Modules

- **Pmod™ devices** are Digilent's line of small I/O interface boards.
  - That offer an ideal way to extend the capabilities of programmable logic and embedded control boards.
- Pmod modules communicate with system boards using 6, 8, or 12-pin connectors.

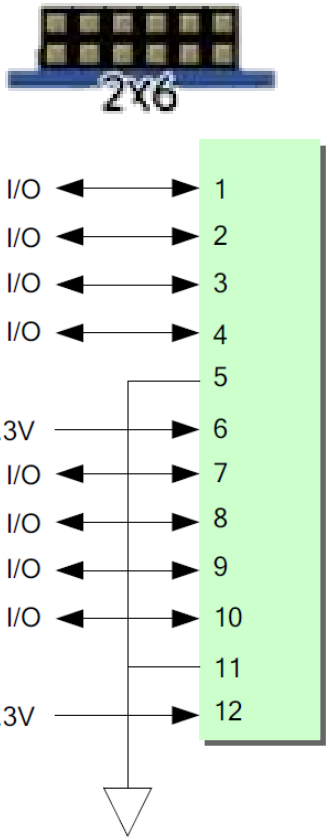




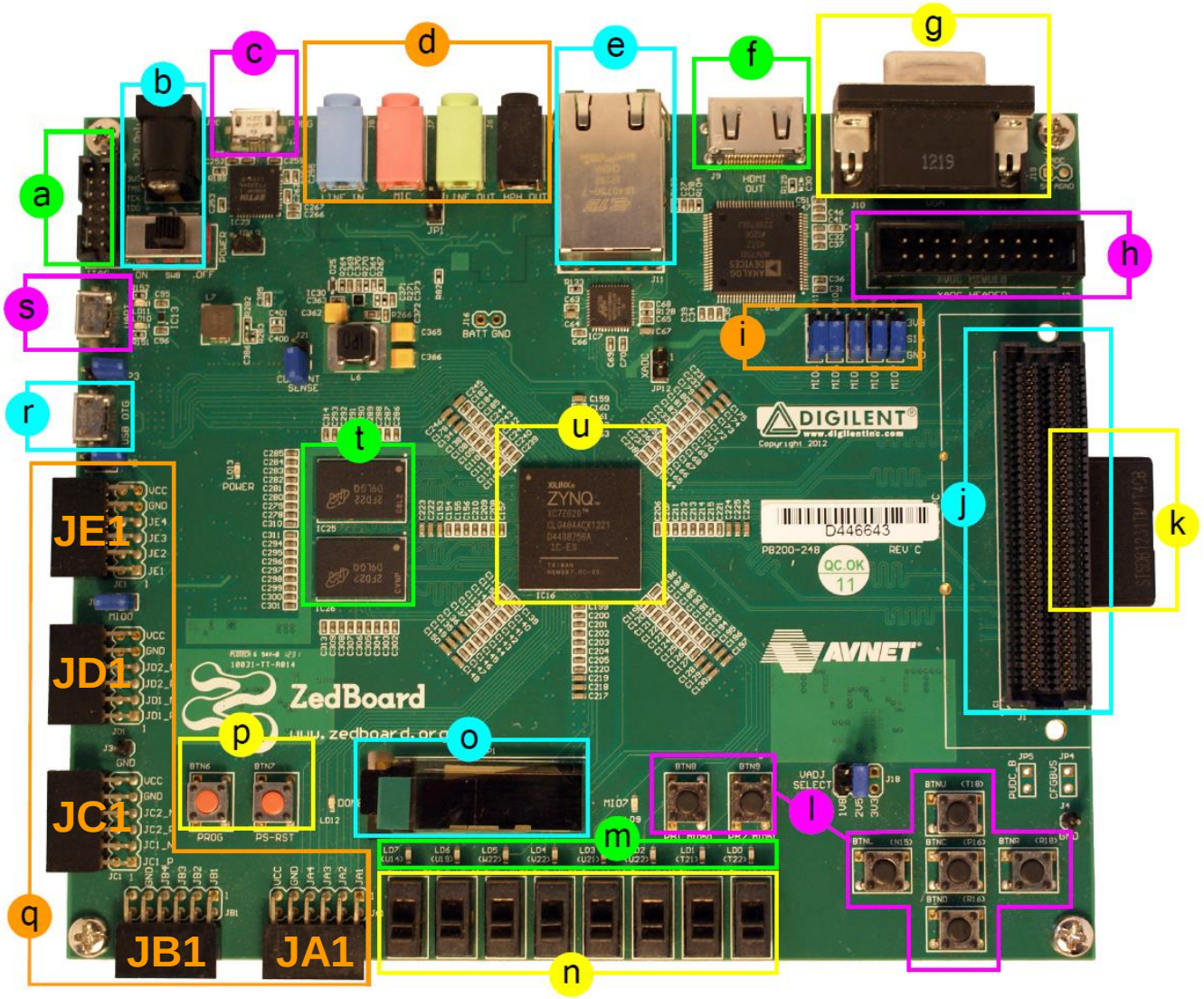
https://store.digilentinc.com/pmod-modules-connectors/

Pmod Ports on ZedBoard (1/3)

- ZedBoard has five Pmod™ compatible headers (**2x6**).

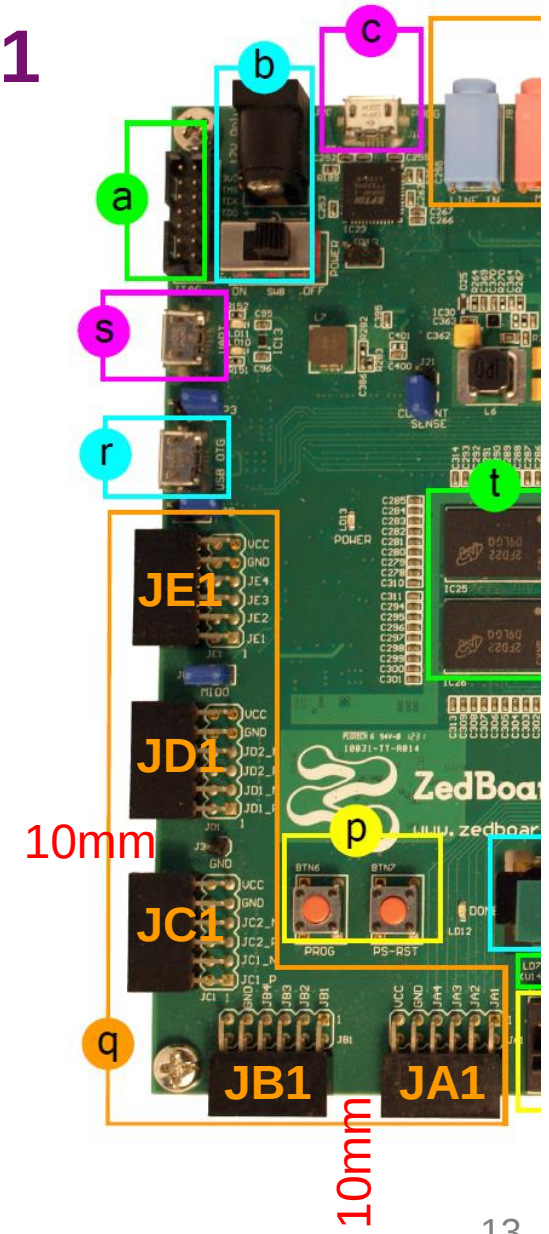


Eight user I/O
Two 3.3V signals
Two ground signals



Pmod Ports on ZedBoard (2/3)

- *Four* Pmod connectors (**JA1, JB1, JC1** and **JD1**) interface to the **PL-side** of the Zynq-7000 AP SoC.
  - **JA1~JD1** connect to Bank 13 (3.3V).
  - **JA1~JD1** are placed in adjacent pairs on the board edge.
    - The clearance between JA1 and JB1 and between JC1 and JD1 are both 10mm.
  - **JC1** and **JD1** are aligned in a dual configuration and routed differentially.
    - To support LVDS running at 525Mbs.
- Pmod (**JE1**) connects to the **PS-side** on MIO pins [0,9-15] in MIO Bank 0/500 (3.3V).



Pmod Ports on ZedBoard (3/3)

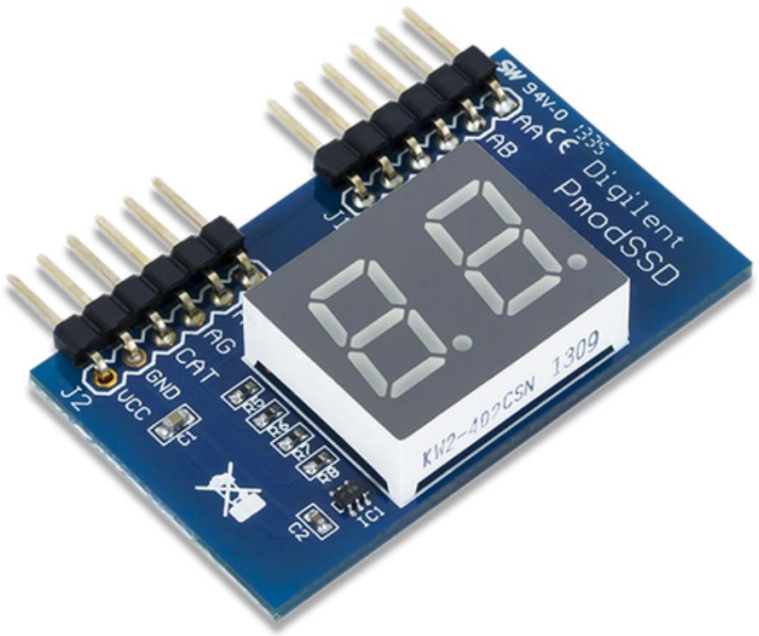
Pmod	Signal Name	Zynq pin	Pmod	Signal Name	Zynq pin
JA1	JA1	Y11	JB1	JB1	W12
	JA2	AA11		JB2	W11
	JA3	Y10		JB3	V10
	JA4	AA9		JB4	W8
	JA7	AB11		JB7	V12
	JA8	AB10		JB8	W10
	JA9	AB9		JB9	V9
	JA10	AA8		JB10	V8

Pmod	Signal Name	Zynq pin	Pmod	Signal Name	Zynq pin
JC1 Differential	JC1_N	AB6	JD1 Differential	JD1_N	W7
	JC1_P	AB7		JD1_P	V7
	JC2_N	AA4		JD2_N	V4
	JC2_P	Y4		JD2_P	V5
	JC3_N	T6		JD3_N	W5
	JC3_P	R6		JD3_P	W6
	JC4_N	U4		JD4_N	U5
	JC4_P	T4		JD4_P	U6

Pmod	Signal Name	Zynq pin	MIO
JE1 MIO Pmod	JE1	A6	MIO13
	JE2	G7	MIO10
	JE3	B4	MIO11
	JE4	C5	MIO12
	JE7	G6	MIO0
	JE8	C4	MIO9
	JE9	B6	MIO14
	JE10	E6	MIO15

http://zedboard.org/sites/default/files/documentations/ZedBoard_HW_UG_v2_2.pdf

Example: Pmod Seven Segment Display



Digilent

Pmod SSD: Seven-segment Display

$6.99

SKU:
410-126

Current Stock:
158

Support Materials

Datasheet

Schematics (PDF)

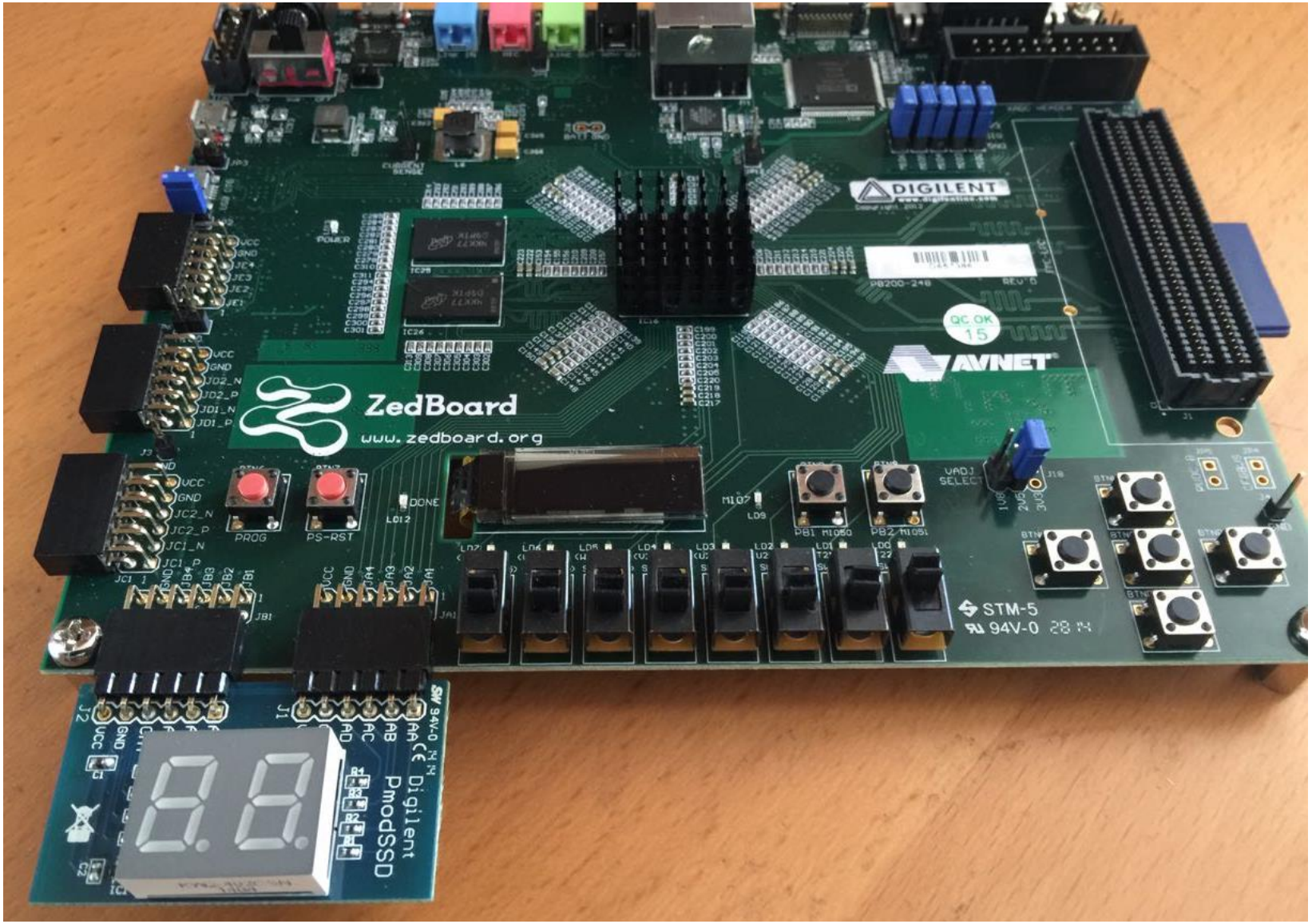
For all other material:

Resource Center

- Product Description
  - The Pmod SSD is a two-digit seven-segment display.
  - Users can toggle through GPIO signals which digit is currently on at a rate of 50 Hz or greater.
    - To achieve persistence-of-vision to give the effect of both digits being lit up simultaneously.

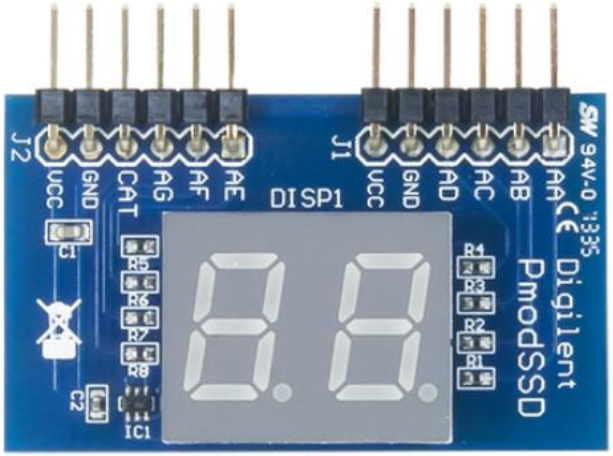
https://store.digilentinc.com/pmod-ssd-seven-segment-display/

Pmod SSD: Connect to ZedBoard



Pmod SSD: Time Multiplexing

- The two-digit displays share the same seven pins to control the seven segments of each display
  - One pin (e.g., **`sel`**) is to select which display to drive.



- To display both digits, we need to alternate between the two digits faster than the eye can perceive.
  - It look like both digits are displayed at the same time.
  - For example, activate the 7-segment on the right then left at a rate of 50 Hz and so on. (how to?)

Pmod SSD: Pinout Description Table

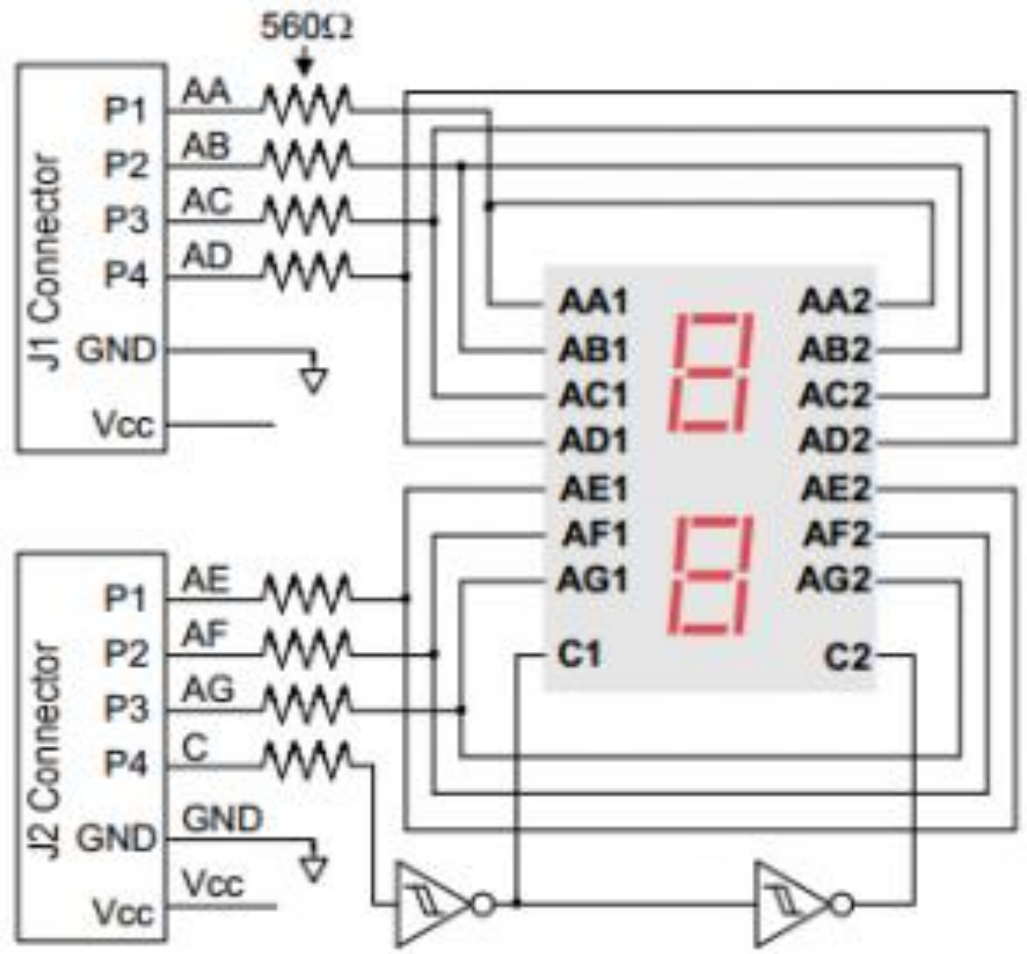
Header J1		
Pin	**Signal**	**Description**
1	AA	Segment A
2	AB	Segment B
3	AC	Segment C
4	AD	Segment D
5	GND	Power Supply Ground
6	VCC	Positive Power Supply

ssd

Header J2		
Pin	**Signal**	**Description**
1	AE	Segment E
2	AF	Segment F
3	AG	Segment G
4	C	Digit Selection pin
5	GND	Power Supply Ground
6	VCC	Positive Power Supply

ssd

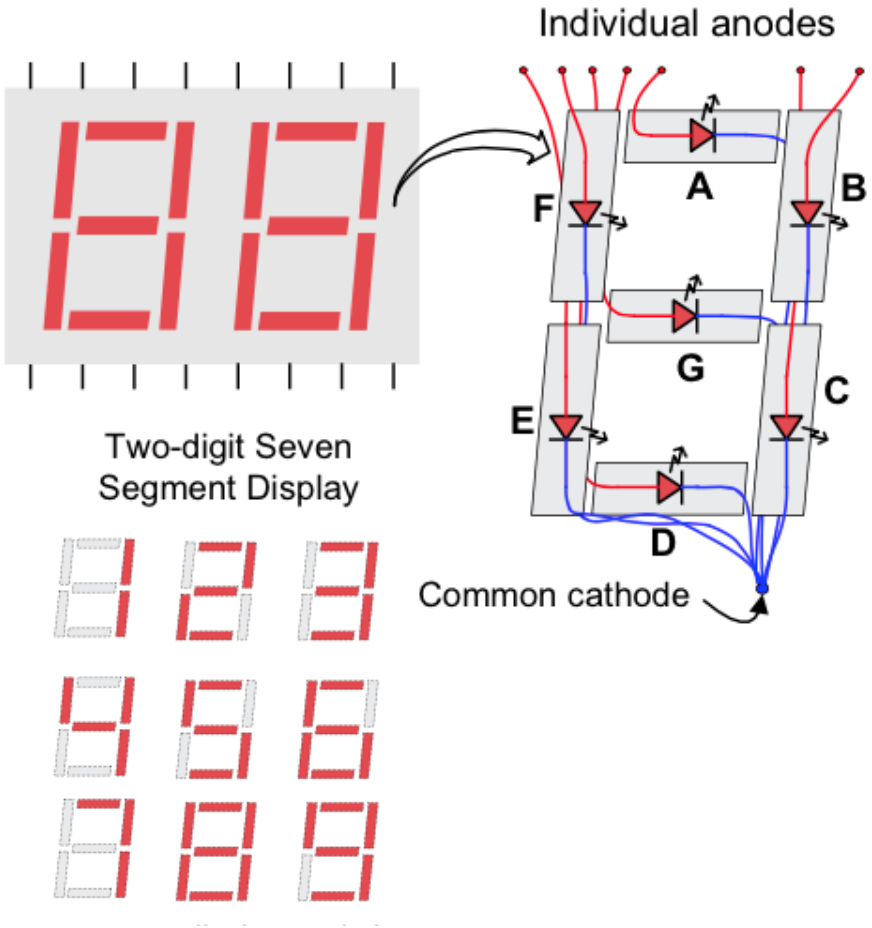
sel



https://store.digilentinc.com/pmod-ssd-seven-segment-display/

Pmod SSD: LED Mapping and Activation

- Each digit has seven LEDs, labeled **A** through **G**.
- To make the digits? Activating LED values as below:



Digit	Segments	Value (ssd)
0	A B C D E F	"1111110"
1	B C	"0110000"
2	A B D E G	"1101101"
3	A B C D G	"1111001"
4	B C F G	"0110011"
5	A C D F G	"1011011"
6	A C D E F G	"1011111"
7	A B C	"1110000"
8	A B C D E F G	"1111111"
9	A B C F G	"1110011"

Pmod SSD: XDC Constraint File

- To drive the Pmod SSD, you also need the following:

Seven Segments (ssd)

```
set_property IOSTANDARD LVCMOS33 [get_ports ssd]
set_property PACKAGE_PIN Y11  [get_ports {ssd[6]}]
set_property PACKAGE_PIN AA11 [get_ports {ssd[5]}]
set_property PACKAGE_PIN Y10  [get_ports {ssd[4]}]
set_property PACKAGE_PIN AA9  [get_ports {ssd[3]}]
set_property PACKAGE_PIN W12  [get_ports {ssd[2]}]
set_property PACKAGE_PIN W11  [get_ports {ssd[1]}]
set_property PACKAGE_PIN V10  [get_ports {ssd[0]}]
```

Digit Selection (sel)

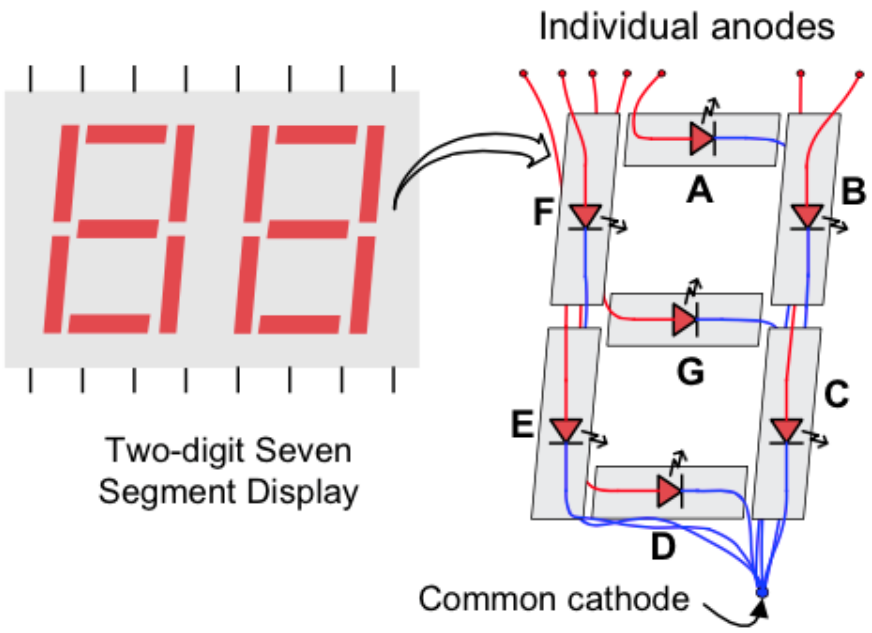
```
set_property IOSTANDARD LVCMOS33 [get_ports sel]
set_property PACKAGE_PIN W8 [get_ports sel]
```

Pmod	Signal Name	Zynq pin	Pmod	Signal Name	Zynq pin
JA1	JA1	Y11	JB1	JB1	W12
	JA2	AA11		JB2	W11
	JA3	Y10		JB3	V10
	JA4	AA9		JB4	W8
	JA7	AB11		JB7	V12
	JA8	AB10		JB8	W10
	JA9	AB9		JB9	V9
	JA10	AA8		JB10	V8

Class Exercise 6.2

Student ID: _____ Date:
Name: _____ _____

- Show how to activate the LED values (**ssd**) for hexadecimal digits:
  A, b, C, d, E, F.



Digit	Segments	Value (ssd)
0	A B C D E F	"1111110"
1	B C	"0110000"
2	A B D E G	"1101101"
3	A B C D G	"1111001"
4	B C F G	"0110011"
5	A C D F G	"1011011"
6	A C D E F G	"1011111"
7	A B C	"1110000"
8	A B C D E F G	"1111111"
9	A B C F G	"1110011"
A		
b		
C		
d		
E		
F		

Summary

- Clock Sources of ZedBoard

- Digilent Pmod™ Peripheral Modules
  - Example: Seven Segment Display (Pmod SSD)